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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/082,055	02/26/2002	Kohtaroh Gotoh	100021-00072	5415

7590 05/17/2004

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EXAMINER	
RAYMOND, EDWARD	
ART UNIT	**PAPER NUMBER**
2857	

DATE MAILED: 05/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/082,055	GOTOH ET AL.	
	Examiner	Art Unit	
	Edward Raymond	2857	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 03 June 2002.

2a)☐ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-44 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,5-11,13,15,21-23,25-31,33,41 and 43 is/are rejected.

7)☒ Claim(s) 4,12,14,16-20,24,32,34-40,42 and 44 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 30 June 2002 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 20040213
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. **Claims 8 and 28** are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. The term "fixed" in the text of the claim is unclear.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. **Claims 1-3, 6-11, 13, 21-23, 26-31, 33, 41, and 43** are rejected under 35 U.S.C. 102(b) as being anticipated by Whetsel, Jr. Whetsel Jr. teaches a test circuit that is incorporated in a device having an output circuit for outputting a signal (Claims 1, 21, 41, and 43: see Figure 1: Integrated Circuit 10: OUT1-OUT4 16), and that carries out a verification of a connection of nodes of said device (Claims 1, 21, 41, and 43: see col. 5, lines 48-60: The Examiner notes that the verification of the integrity of the overall boundary scan path is equivalent to the verification of a connection of nodes or circuits), said test circuit comprising a test data generating circuit generating test data for carrying out a verification of a connection of output nodes of said output circuit (Claims 1, 21, 41, and 43: see col. 5, lines 39-50: The Examiner notes that the self-test function of the test

circuit has to generate the same signals that would be generated from the control bus during external test operations); and a test output buffer, connected in parallel with said output nodes (Claims 1, 21, 41, and 43: see Figure 13: Output Buffer 236 and also Figure 14: The Examiner notes that the output buffer is indirectly in parallel to the output nodes of DOUT), receiving test data from said test data generating circuit (Claims 1, 21, 41, and 43: see col. 3, lines 13-16) and outputting the test data to said output nodes (Claims 1, 21, 41, and 43: see Figure 13: Output Buffer 236 and also Figure 14).

Whetsel, Jr. teaches a test circuit wherein said output circuit outputs a differential signal (Claims 2 and 22: see Figure 1: OUT1-OUT4: The Examiner notes that the outputs from the test cell, which includes combinational logic circuitry, are differential signals), and said test output buffer outputs said test data to said differential output nodes (Claims 2 and 22: see Figure 1: see Output Buffer 20).

Whetsel, Jr. teaches a test circuit wherein said test circuit carries out the verification of the connection of said output nodes in a differential signal status (Claims 3 and 23: see col. 14, lines 59-63: The Examiner notes that the comparator is used to test the circuits and determine the functionality of the circuit based on comparison to output a verification output).

Whetsel, Jr. teaches a test circuit wherein said test data generating circuit is constructed of a circuit that has a register function capable of performing scanning (Claims 6 and 26: see col. 18, lines 55-62).

Whetsel, Jr. teaches a test circuit wherein a test clock, which is different from an operation clock of said output circuit, is supplied to said test data generating circuit

(Claims 7 and 27: see Figures 13 and 14: CLK and PSA/PRPG Test Clock, respectively)

Whetsel, Jr. teaches a test circuit wherein said test data generating circuit outputs test data which is fixed to the verification of the connection of said output nodes (Claims 8 and 28: see col. 5, lines 39-50: The Examiner notes that the self-test feature is equivalent to being fixed).

Whetsel, Jr. teaches a test circuit wherein an output of said output circuit is provided with a terminating resistor (Claims 9 and 29: see Figure 1: Output Buffer 20: The Examiner notes that the output buffer has resistance and performs the equivalent function of a terminating resistor).

Whetsel, Jr. teaches a test circuit wherein said test output buffer directly controls said output circuit (Claims 10 and 30: see Figure 1: Output Buffer 20 and OUT1-OUT4 16).

Whetsel, Jr. teaches a test circuit further comprising a test input buffer connected in parallel with input nodes of an input circuit to which a signal is applied (Claims 11 and 31: see Figure 1: Input Buffer 18), and said test input buffer receiving test data that are input to said input nodes (Claims 11 and 31: see Figure 1: DIN 12a-d).

Whetsel, Jr. teaches a test circuit wherein said input circuit receives a differential signal, and said test input buffer receives test data that has been input to said differential input nodes (Claims 13 and 33: see Figure 1: Input Buffer 18).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

7. **Claims 5, 15, and 25** are rejected under 35 U.S.C. 103(a) as being unpatentable over Whetsel, Jr. in view of Malladi.

8. Whetset, Jr. teaches all of the features of the claimed invention, except a test circuit wherein when said output circuit has a function of converting parallel data into serial data, said test data generating circuit also has a function of converting parallel data into serial data. Malladi teaches a serializer and deserializer (Claims 5, 15, and 25: see col. 5, lines 34-45). It would have been obvious to the person having ordinary skill in the art at the time the invention was made to modify Whetsel, Jr. to use a serializer and a deserializer, as taught by Malladi, because this would allow for the

transmission and reception of the correct protocol of the input standard of the combinational logic circuit in use.

Allowable Subject Matter

9. **Claims 4, 12, 14, 16-20, 24, 32, 34-40, 42, and 44** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

10. **Claims 8 and 28** would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

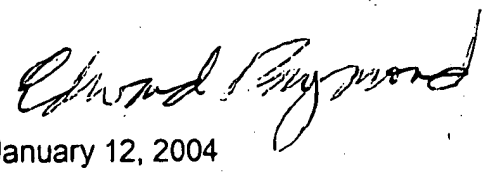
11. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Contact Information

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Edward Raymond whose telephone number is 703-308-6235 until January 26, 2004 and 571-272-2221 thereafter. The examiner can normally be reached on Monday through alternating Friday between 8:00 AM and 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc Hoff can be reached on 703-308-1677. The fax phone numbers for the organization where this application or proceeding is assigned are 703-746-4447 for regular communications and 703-308-0956 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-1782.



January 12, 2004
Edward Raymond
Patent Examiner
Art Unit 2857